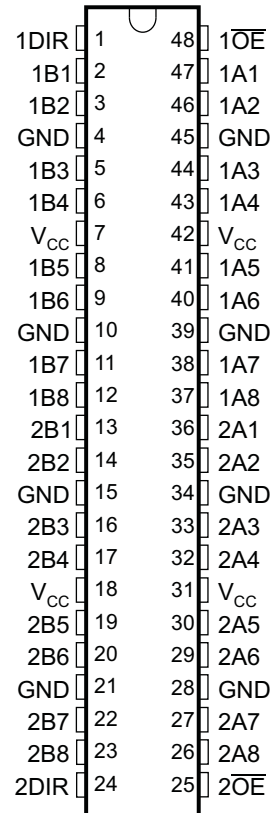


FEATURES

- **Controlled Baseline**
 - One Assembly
 - One Test Site
 - One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **Member of the Texas Instruments Widebus™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN74LVTH16245A-EP

3.3-V ABT 16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCAS693G—APRIL 2003—REVISED OCTOBER 2006

DESCRIPTION/ORDERING INFORMATION

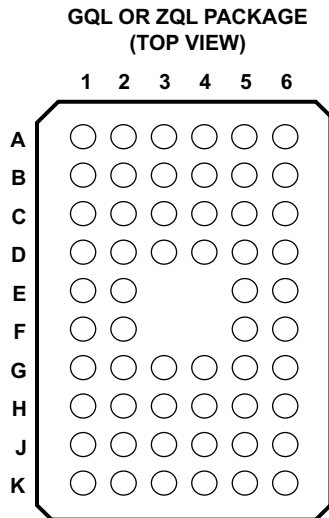
The SN74LVTH16245A is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the devices so that the buses effectively are isolated.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 V and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



TERMINAL ASSIGNMENTS⁽¹⁾

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|------|-----|----------|----------|------|-------------------|
| A | 1DIR | NC | NC | NC | NC | 1 \overline{OE} |
| B | 1B2 | 1B1 | GND | GND | 1A1 | 1A2 |
| C | 1B4 | 1B3 | V_{CC} | V_{CC} | 1A3 | 1A4 |
| D | 1B6 | 1B5 | GND | GND | 1A5 | 1A6 |
| E | 1B8 | 1B7 | | | 1A7 | 1A8 |
| F | 2B1 | 2B2 | | | 12A2 | 2A1 |
| G | 2B3 | 2B4 | GND | GND | 2A4 | 2A3 |
| H | 2B5 | 2B6 | V_{CC} | V_{CC} | 2A6 | 2A5 |
| J | 2B7 | 2B8 | GND | GND | 2A8 | 2A7 |
| K | 2DIR | NC | NC | NC | NC | 2 \overline{OE} |

(1) NC – no internal connection

ORDERING INFORMATION

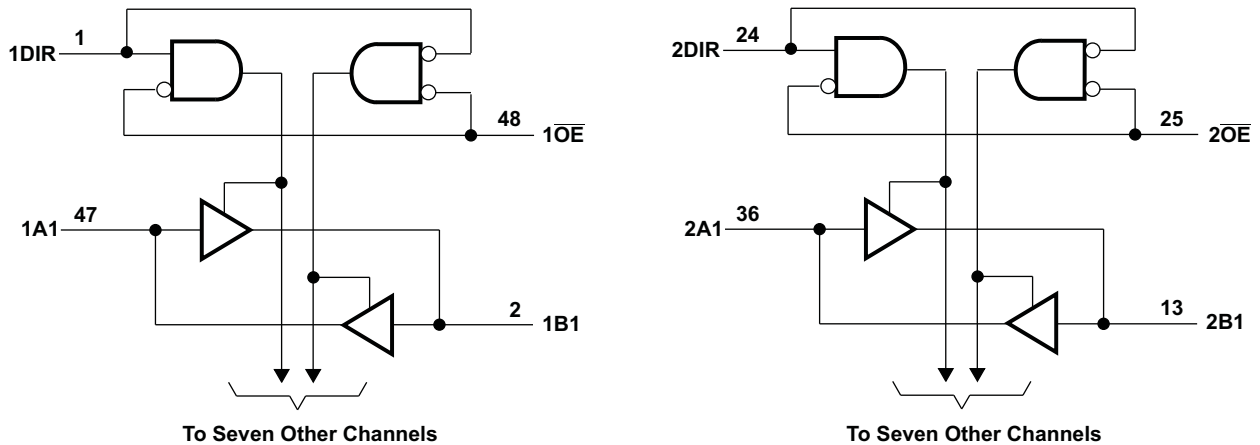
| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|--------------------------|---------------|-----------------------|------------------|
| –40°C to 125°C | SSOP – DL | Tape and reel | CLVTH16245AQDLREP | LH16245AEP |
| | TSSOP – DGG | Tape and reel | CLVTH16245AQDGGREP | LH16245AEP |
| –40°C to 85°C | TVSOP – DGV | Tape and reel | CLVTH16245AIDGVREP | LL245AEP |
| | VFBGA – GQL | Tape and reel | CLVTH16245AIGQLREP | LL245AEP |
| | VFBGA – ZQL (Pb-free) | | CLVTH16245AIZQLREP | |
| –55°C to 125°C | SSOP – DL | Tape and reel | CLVTH16245AMDREP | LH16245AEP |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 8-bit section)

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|---------------------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 4.6 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 7 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 7 | V |
| V_O | Voltage range applied to any output in the high state ⁽²⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_O | Current into any output in the low state | SN74LVTH16245A(Q/M) | 96 | mA |
| | | SN74LVTH16245AI | 128 | |
| I_O | Current into any output in the high state ⁽³⁾ | SN74LVTH16245A(Q/M) | 48 | mA |
| | | SN74LVTH16245AI | 64 | |
| I_{IK} | Input clamp current | $V_I < 0$ | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DGG package | 70 | °C/W |
| | | DGV package | 58 | |
| | | DL package | 63 | |
| | | GQL/ZQL package | 42 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- This current flows only when the output is in the high state and $V_O > V_{CC}$.
- The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVTH16245A-EP
3.3-V ABT 16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCAS693G–APRIL 2003–REVISED OCTOBER 2006

Recommended Operating Conditions⁽¹⁾

| | | SN74LVTH16245AQ | | SN74LVTH16245AI | | SN74LVTH16245AM | | UNIT |
|---------------------|------------------------------------|-----------------|-----|-----------------|-----|-----------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2.7 | 3.6 | 2.7 | 3.6 | 2.7 | 3.6 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | | 0.8 | V |
| V _I | Input voltage | | 5.5 | | 5.5 | | 5.5 | V |
| I _{OH} | High-level output current | | –24 | | –32 | | –24 | mA |
| I _{OL} | Low-level output current | | 24 | | 64 | | 24 | mA |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | 10 | 10 | 10 | 10 | ns/V |
| Δt/ΔV _{CC} | Power-up ramp rate | 200 | | 200 | | 200 | | μs/V |
| T _A | Operating free-air temperature | –40 | 125 | –40 | 85 | –55 | 125 | °C |

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN74LVTH16245AQ | | | SN74LVTH16245AI | | | SN74LVTH16245AM | | | UNIT | | |
|-------------------------------------|--|---|--|----------------------|---------|-----------------|--------------------|--------------------------|-----------------|--------------------|-----|---------------|---------------|---------------|
| | | | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP ⁽¹⁾ | MAX | | | |
| V_{IK} | | $V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$ | -1.2 | | | -1.2 | | | -1.2 | | | V | | |
| V_{OH} | | $V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$ | $V_{CC} - 0.2$ | | | $V_{CC} - 0.2$ | | | $V_{CC} - 0.2$ | | | V | | |
| | | $V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$ | 2.4 | | | 2.4 | | | 2.4 | | | | | |
| | | $V_{CC} = 3.3\text{ V}$ | $I_{OH} = -24\text{ mA}$ | | 2 | | | $I_{OH} = -32\text{ mA}$ | | 2 | | | | |
| V_{OL} | | $V_{CC} = 2.7\text{ V}$ | $I_{OL} = 100\text{ }\mu\text{A}$ | | 0.2 | | | $I_{OL} = 24\text{ mA}$ | | 0.5 | | | V | |
| | | | $I_{OL} = 24\text{ mA}$ | | 0.5 | | | $I_{OL} = 16\text{ mA}$ | | 0.4 | | | | |
| | | $V_{CC} = 3\text{ V}$ | $I_{OL} = 16\text{ mA}$ | | 0.4 | | | $I_{OL} = 32\text{ mA}$ | | 0.5 | | | | |
| | | | $I_{OL} = 32\text{ mA}$ | | 0.5 | | | $I_{OL} = 64\text{ mA}$ | | 0.55 | | | | |
| | | | $I_{OL} = 64\text{ mA}$ | | 0.55 | | | | | | | | | |
| I_I | | Control inputs | $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND | | ± 1 | | | ± 1 | | ± 1 | | | μA | |
| | | | $V_{CC} = 0$ or 3.6 V , $V_I = 5.5\text{ V}$ | | 10 | | | 10 | | 10 | | | | |
| | | A or B port ⁽²⁾ | $V_{CC} = 3.6\text{ V}$ | $V_I = 5.5\text{ V}$ | | 20 | | | 20 | | 20 | | | |
| | | | | $V_I = V_{CC}$ | | 5 | | | 1 | | 5 | | | |
| | | | $V_I = 0$ | | -5 | | | -5 | | -5 | | | | |
| I_{off} | | $V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V | | | | ± 100 | | | | | | μA | | |
| $I_{I(\text{hold})}$ ⁽³⁾ | | A or B port | $V_{CC} = 3\text{ V}$ | $V_I = 0.8\text{ V}$ | | 75 | | | 75 | | 75 | | | μA |
| | | | | $V_I = 2\text{ V}$ | | -75 | | | -75 | | -75 | | | |
| | | $V_{CC} = 3.6\text{ V}$, $V_I = 0$ to 3.6 V | | | | | 500 | | | -750 | | | | |
| I_{OZPU} | | $V_{CC} = 0$ to 1.5 V , $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$ | ± 100 | | | ± 100 | | | ± 100 | | | μA | | |
| I_{OZPD} | | $V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$ | ± 100 | | | ± 100 | | | ± 100 | | | μA | | |
| I_{CC} | | $V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND | Outputs high | | 0.19 | | | 0.19 | | 0.19 | | | mA | |
| | | | Outputs low | | 5 | | | 5 | | 5 | | | | |
| | | | Outputs disabled | | 0.19 | | | 0.19 | | 0.19 | | | | |
| ΔI_{CC} ⁽⁴⁾ | | $V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND | 0.2 | | | 0.2 | | | 0.2 | | | mA | | |
| C_i | | $V_I = 3\text{ V or } 0$ | 4 | | | 4 | | | 4 | | | pF | | |
| C_{io} | | $V_O = 3\text{ V or } 0$ | 10 | | | 10 | | | 10 | | | pF | | |

 (1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

 (2) Unused pins at V_{CC} or GND

(3) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 (4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

SN74LVTH16245A-EP

3.3-V ABT 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS693G–APRIL 2003–REVISED OCTOBER 2006

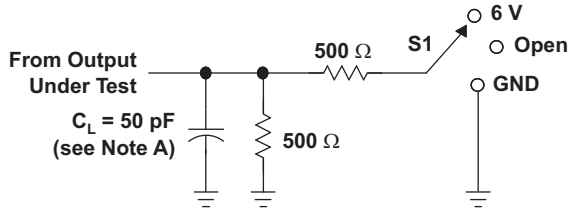
Switching Characteristics

over operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVTH16245AQ SN74LVTH16245AM | | | | SN74LVTH16245AI | | | | UNIT | |
|-------------|-----------------|----------------|---|-----|-------------------------|-----|---|--------------------|-----|-------------------------|------|-----|
| | | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP ⁽¹⁾ | MAX | MIN | | MAX |
| t_{PLH} | A or B | B or A | 0.5 | 4.5 | 4.6 | | 1.5 | 2.3 | 3.3 | 3.7 | | ns |
| t_{PHL} | | | 0.5 | 4.4 | 3.9 | | 1.3 | 2.1 | 3.3 | 3.5 | | |
| t_{PZH} | \overline{OE} | A or B | 0.5 | 6.5 | 6.6 | | 1.5 | 2.8 | 4.5 | 5.3 | | ns |
| t_{PZL} | | | 0.5 | 5.4 | 6.2 | | 1.6 | 2.9 | 4.6 | 5.2 | | |
| t_{PHZ} | \overline{OE} | A or B | 1 | 6.8 | 7 | | 2.3 | 3.7 | 5.1 | 5.5 | | ns |
| t_{PLZ} | | | 1 | 6.2 | 6.3 | | 2.2 | 3.5 | 5.1 | 5.4 | | |
| $t_{sk(o)}$ | | | | | | | | 0.5 | | 0.5 | ns | |

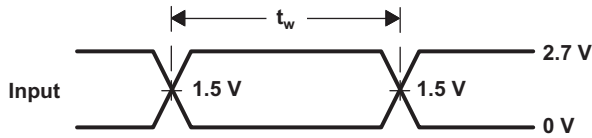
(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

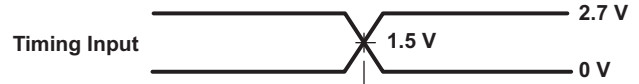


LOAD CIRCUIT

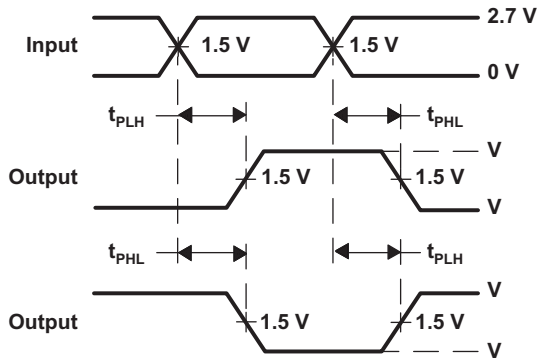
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



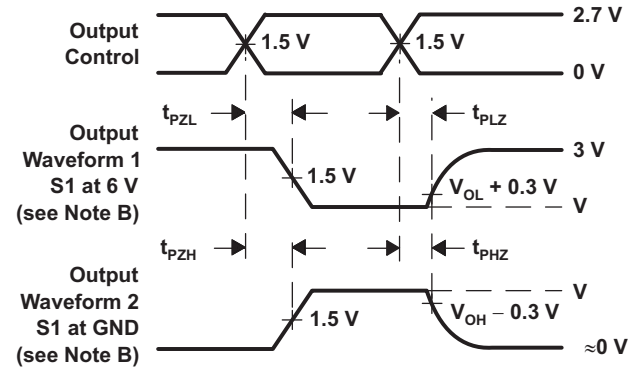
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 59 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|-----------------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 8V16245AMDLEPG4 | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CLVTH16245AIDGVREP | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CLVTH16245AIZQLREP | ACTIVE | BGA MI CROSTAR JUNIOR | ZQL | 56 | 1000 | Pb-Free (RoHS) | SNAGCU | Level-1-260C-UNLIM |
| CLVTH16245AMDLEP | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CLVTH16245AQDGGREP | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CLVTH16245AQDLREP | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04602-01XE | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04602-01YE | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04602-02UA | ACTIVE | BGA MI CROSTAR JUNIOR | GQL | 56 | | TBD | Call TI | Call TI |
| V62/04602-02ZE | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04602-03XE | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVTH16245A-EP :

- Catalog: [SN74LVTH16245A](#)
- Automotive: [SN74LVTH16245A-Q1](#)
- Military: [SN54LVTH16245A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CLVTH16245AIDGVREP | TVSOP | DGV | 48 | 2000 | 330.0 | 24.4 | 6.8 | 10.1 | 1.6 | 12.0 | 24.0 | Q1 |
| CLVTH16245AIZQLREP | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 330.0 | 16.4 | 4.8 | 7.3 | 1.45 | 8.0 | 16.0 | Q1 |
| CLVTH16245AMDREP | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |
| CLVTH16245AQDGGREP | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |
| CLVTH16245AQDLREP | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

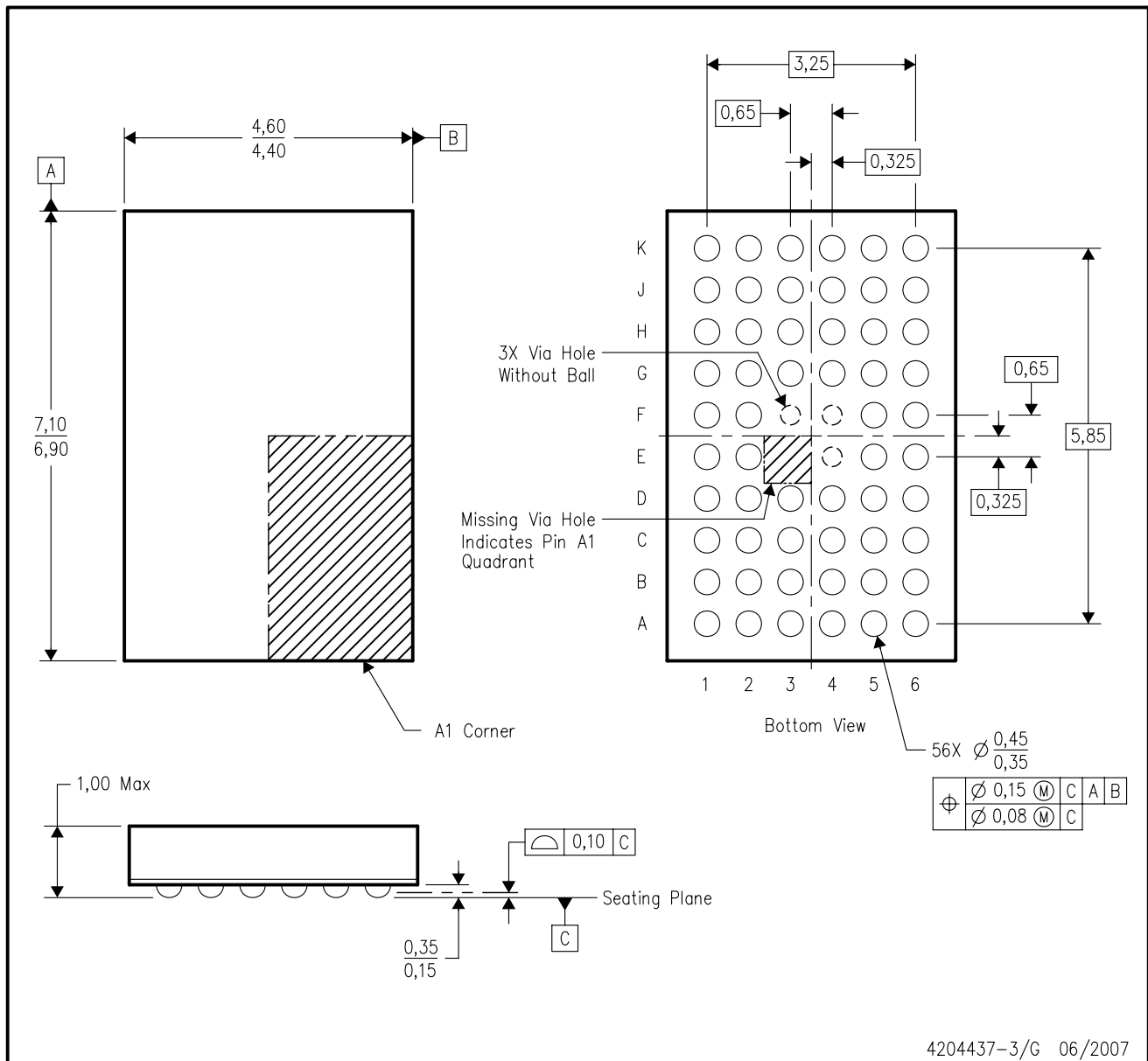


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| CLVTH16245AIDGVREP | TVSOP | DGV | 48 | 2000 | 346.0 | 346.0 | 41.0 |
| CLVTH16245AIZQLREP | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 346.0 | 346.0 | 33.0 |
| CLVTH16245AMDREP | SSOP | DL | 48 | 1000 | 346.0 | 346.0 | 49.0 |
| CLVTH16245AQDGGREP | TSSOP | DGG | 48 | 2000 | 346.0 | 346.0 | 41.0 |
| CLVTH16245AQLREP | SSOP | DL | 48 | 1000 | 346.0 | 346.0 | 49.0 |

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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